Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. Amultiplying digital-to-analog converter (MDAC) stage for a pipelined analog-to-digital converter, the MDAC stage comprising:

an input node for receiving an analog signal;

a sub-analog-to-digital converter for converting the analog signal to a digital code;

an amplifier;

a first capacitance selectively connected between the input node and the amplifier input and between the amplifier input and the amplifier output; and

a plurality of second capacitances in parallel selectively connected between the input node and the amplifier input and between a corresponding plurality of digital reference signals and the amplifier input, the plurality of digital reference signals comprising digital signals corresponding to the digital code and a first calibration signal;

wherein during a sample phase the first capacitance is connected between the input node and the amplifierinput and the plurality of second capacitances are connected in parallel between the input node and the ampli-

fier input, and during a hold phase the first capacitance is connected between the amplifier input and the amplifieroutput and the plurality of second capacitances are connected in parallel between the plurality of digital reference signals and the amplifier input.

[c2] 2. The MDAC stage of claim 1 wherein the sum of the plurality of second capacitances is nominally equal to the first capacitance.

[c3] 3. A pipelined analog-to-digital converter comprising a series of MDAC stages of claim 1.

[c4] 4. The pipelined analog-to-digital converter of claim 3 further comprising:

a multiplier connected to the output of the last MDAC stage of the series, the multiplier for determining a product of the last MDAC stage output anda second calibration signal corresponding to the first calibration signal;

a low-pass filterconnected to the multiplier for filtering output of the multiplier and outputting a DC component; and

an encoder for receiving output of the MDAC stages and generating a digital output signal, and for compensating the digital output signal with the DC component.

[c5] 5. The pipelined analog-to-digital converter of claim 4 wherein the first and second calibration signals are random digitalbinary-valued sequences having the same waveform shape.

[c6] 6. The pipelined analog-to-digital converter of claim 4 further comprising a pseudo-random signal generator for generating the first and second calibration signals.

[c7] 7. The pipelined analog-to-digital converter of claim 4 further comprising a memory for storing the DC component, the memory accessible by the encoder.

[c8] 8. A method for background calibrating a pipelined analog-to-digital converter comprising a series of multiplying digital-to-analog converter (MDAC) stages, the method comprising:
sampling an input analog signal on a first capacitance and a plurality of second capacitances of an MDAC stage during a sample phase;
applying a first calibration signal to a second capacitance of the MDAC stage during a hold phase;
combining output of the last MDAC stage of the series with a second calibration signal corresponding to the first calibration signal; and
filtering the second calibration signal from the digital output of the pipelined analog-to-digital converter.

[c9] 9. The method of claim 8 further comprising sequentially applying the first calibration signal to second capacitances of all MDAC stages during corresponding hold phases, said sequential application being in order of increasing significant bit values of the MDAC stages.

[c10] 10. The method of claim 8 wherein the sum of the plurality of second capacitances is nominally equal to the first capacitance.

[c11] 11. The method of claim 8 where the first and second calibration signals are random digital binary-valued sequences having the same waveform shape.